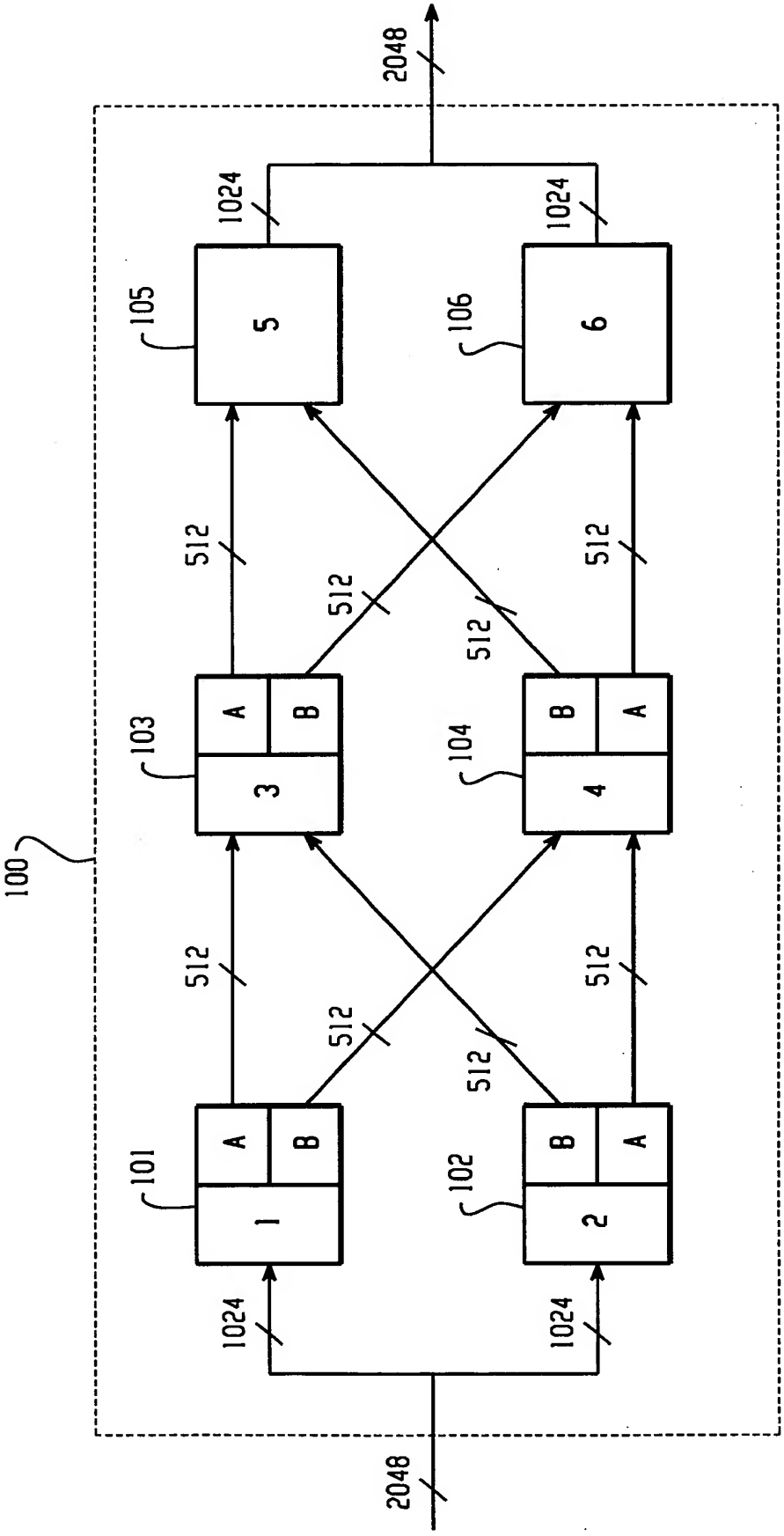
100
2048
1024
1024
105
5
106
6
512
512
512
512
103
A
B
3
104
B
A
4
512
512
512
512
101
A
B
1
102
B
A
2
1024
1024
2048

Fig. 1

	0	1	2	...	4N-1
IN[4N]	4N	4N	4N	...	4N

FIG. 2

Value		Representation
0 to 4N-1	(0x0 - 0x17FF)	Input port # for the matrix
4N	(0x1800)	UNEQ-P
4N+1	(0x1801)	AIS-P

FIG. 3

OUT[][]	0	1	2	...	2N-1
Switch Matrix Unit #1	0	0	0	...	0
Switch Matrix Unit #2	0	0	0	...	0
Switch Matrix Unit #3	0	0	0	...	0
Switch Matrix Unit #4	0	0	0	...	0
Switch Matrix Unit #5	0	0	0	...	0
Switch Matrix Unit #6	0	0	0	...	0

FIG. 4

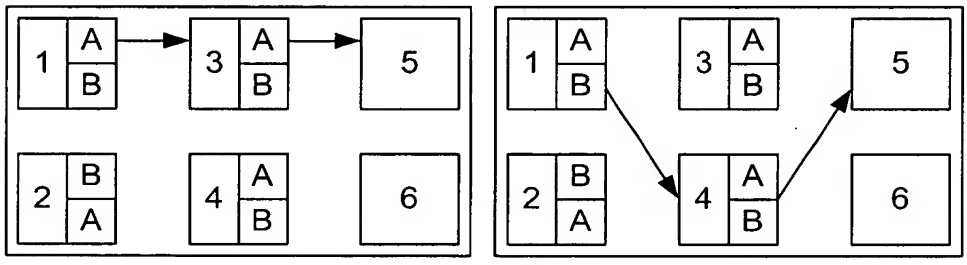

FIG. 5

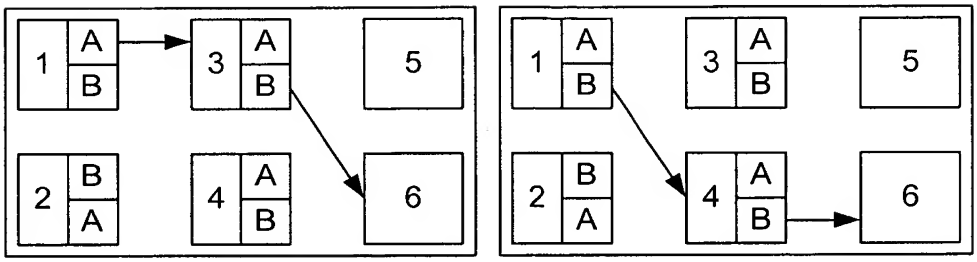

FIG. 6

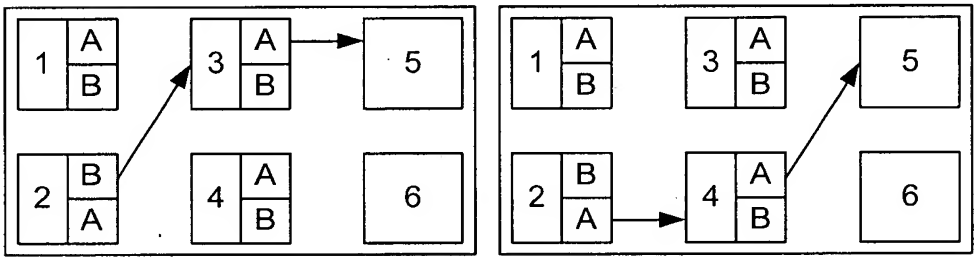

FIG. 7

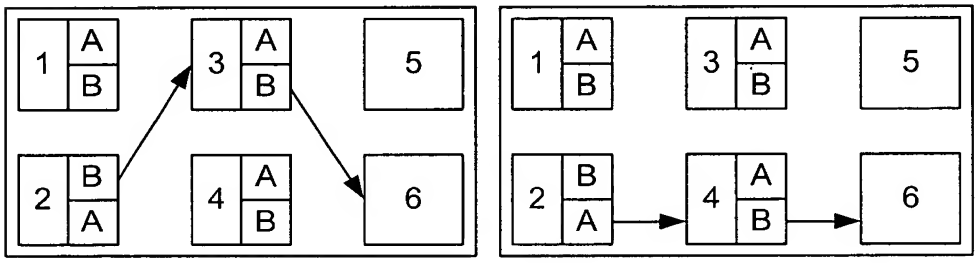

FIG. 8

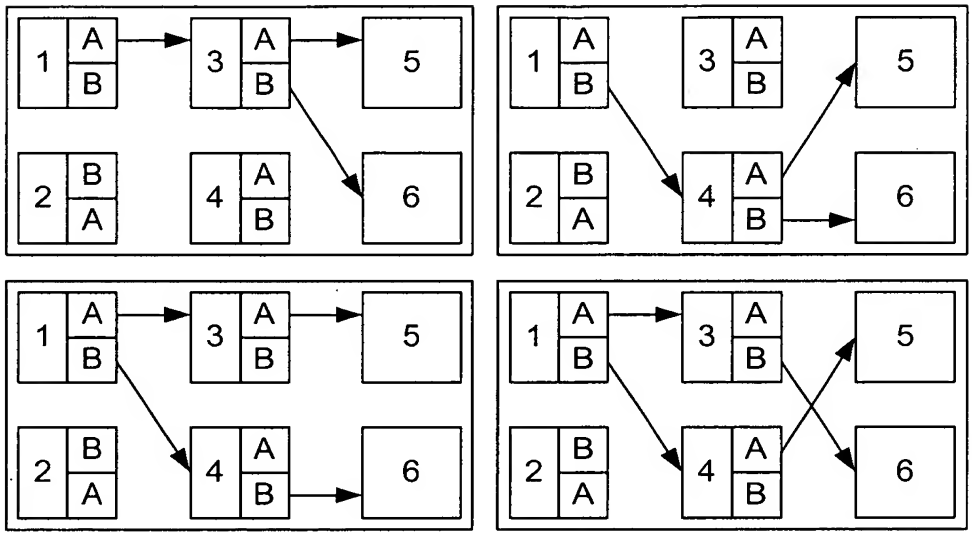

FIG. 9

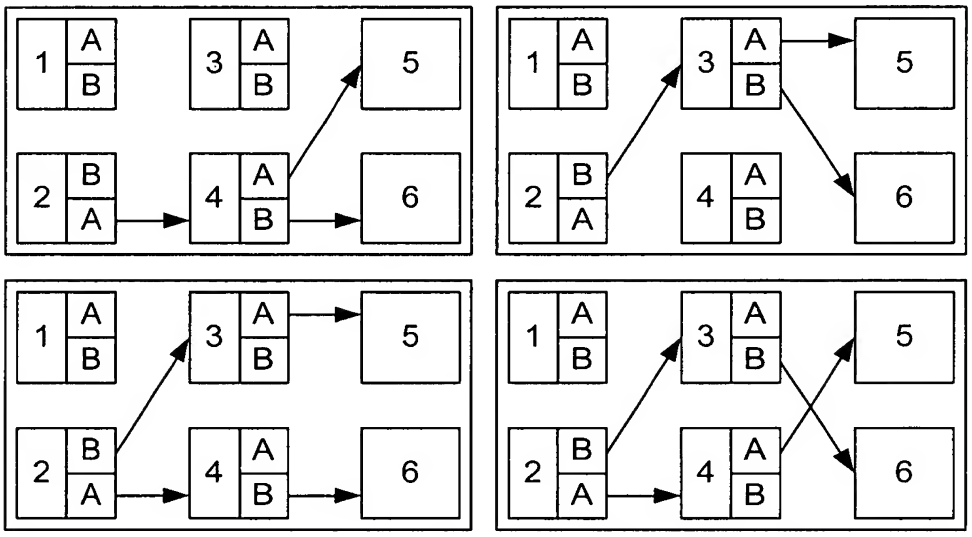

FIG. 10

Input	Switch Matrix Unit #5 Output	Switch Matrix Unit #6 Output
Switch Matrix Unit #1	Preferred: 1A → 3A → 5	Preferred: 1A → 3B → 6
		Alternative: 1B → 4A → 6
	Alternative: 1B → 4B → 5	Preferred: 1B → 4A → 6
		Alternative: 1A → 3B → 6
Switch Matrix Unit #2	Preferred: 2A → 4B → 5	Preferred: 2A → 4A → 6
		Alternative: 2B → 3B → 6
	Alternative: 2B → 3A → 5	Preferred: 2B → 3B → 6
		Alternative: 2A → 4A → 6

FIG. 11

Type of connection	Preferred Path	Alternative Path
Switch Matrix Unit #1 to Switch Matrix Unit #5	1A → 3A → 5	1B → 4B → 5
Switch Matrix Unit #1 to Switch Matrix Unit #6	1B → 4A → 6	1A → 3B → 6
Switch Matrix Unit #2 to Switch Matrix Unit #5	2A → 4B → 5	2B → 3A → 5
Switch Matrix Unit #2 to Switch Matrix Unit #6	2B → 3B → 6	2A → 4A → 6

FIG. 12

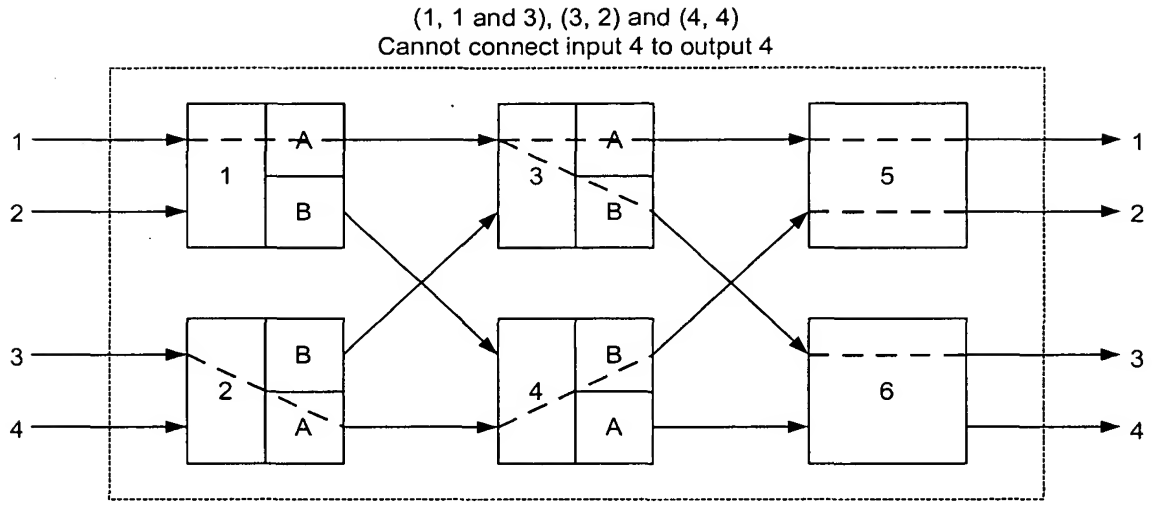

FIG. 13

	Input goes to Switch Matrix Unit #5	Input goes to Switch Matrix Unit #6	Input Captured on Same Switch Matrix Unit	Input Captured on Other Switch Matrix Unit
Input Port # 0	X			
Input Port # 1		X		
Input Port # 2	X	X	X	
. . .	. . .	. . .	. . .	. . .
Input Port # 4N-3		X		
Input Port # 4N-2	X			
Input Port # 4N-1	X	X		X

FIG. 14